IN THE CLAIMS:

Please cancel claims 10-16 without prejudice or disclaimer of the subject matter thereof.

Please add new claim 24 and amend claims 1, 2, 4-7, 17 and 20-23 as follows:

1. (Amended) A DLL (delay locked loop) circuit, comprising:

a delay circuit which is connected to first and second nodes, and which delays an original clock signal supplied to said first node based on a delay control signal and generates first to n-th (n is an integer more than 1) internal clock signals, wherein said first internal clock signal is outputted from said second node, and the internal clock signals other than said first internal clock signal are outputted from said delay circuit without passing through said second node, and lead the first internal clock signal in phase by a predetermined value, and wherein said original clock signal is a frequency variable clock signal and said delay circuit includes a first delay section with a frequency dependent delay time and a second delay section with a fixed delay time;

a phase comparing circuit which compares said original clock signal supplied from said first node and said first internal clock signal supplied from said second node, and outputs a phase difference of said original clock signal and said first internal clock signal; and

a delay control circuit which outputs said delay control signal to said delay circuit based on the phase difference outputted from said phase comparing circuit.

2. (Amended) The DLL circuit according to claim 1, wherein [said delay circuit comprises:]

[a] said first delay section [which] delays said original clock signal based on said delay control signal to generate a first delay signal; and

[a] said second delay section which is provided between said second node and said first delay section, and delays the first delay signal to generate said first to n-th internal clock signals, and outputs said first internal clock signal from said second node, and the internal clock signals other than said first internal clock signal without passing through said second node.

4. (Amended) The DLL circuit according to claim 3, wherein each of said plurality of delay elements [have substantively a same delay quantity] delays said first delay signal by substantially a same amount of time.

5. (Amended) The DLL circuit according to claim 3, wherein each of said plurality of delay elements delays said first delay signal by an amount of time different from other delay elements [have delay quantities different from each other].

6. (Amended) The DLL circuit according to claim 3, wherein an amount of time by which [a delay quantity of] each of said plurality of delay elements delays said first delay signal is predetermined.

7. (Amended) The DLL circuit according to claim 3, wherein [a delay quantity] an amount of time by which [of] each of said plurality of delay elements delays said first delay signal is independent of a frequency of said original clock signal.

17. (Amended) A method of generating timing signals, comprising the steps of:

(a) delaying an original clock signal supplied to a first node based on a delay control signal;

(b) generating first to n-th (n is an integer more than 1) internal clock signals from the delayed original clock signal, wherein said first internal clock signal is outputted from a second node, and the internal clock signals other than said first internal clock signal are outputted without passing through the second node, and lead said first internal clock signal in phase by a predetermined value, and wherein the original clock signal is a frequency variable clock signal, and a first delay section with a frequency dependent delay time and a second delay section with a fixed delay time control delay of the original clock signal and the internal clock signals;

(c) detecting a phase difference between said original clock signal and said first internal clock signal; and

(d) generating said delay control signal based on the detected phase difference.

20. (Amended) The method according to claim 19, wherein each of said plurality of delay elements [have substantively a same delay quantity] delays said first delay signal by substantially a same amount of time.

21. (Amended) The method according to claim 19, wherein each of said plurality of delay elements delays said first delay signal by an amount of time different from other delay elements [have delay quantities different from each other].

22. (Amended) The method according to claim 19, wherein an amount of time by which [a delay quantity of] each of said plurality of delay elements delays said first delay signal is predetermined.

23. (Amended) The method according to claim 19, wherein an amount of time by which [a delay quantity of] each of said plurality of delay elements delays said first delay signal is independent of a frequency of said original clock signal.

24. (New Claim) A synchronous memory, comprising:

a delay locked loop circuit that delays an original clock signal supplied as an input, said delay locked loop circuit producing as an output a plurality of internal clock signals, a first of said plurality of internal clock signals being said original clock signal delayed by a first quantity and a second of said plurality of internal clock signals being said original clock signal delayed by a second quantity different than said first quantity, said delay locked loop circuit comprising:

a variable delay section with a frequency dependent delay time that delays said original clock signal generated as a first delay signal based on a phase difference between said original clock signal and one of said plurality of internal clock signals; and

a fixed delay section that is a multi-stage structure of delay elements that delays said first delay signal by a predetermined amount, said second internal clock signal being generated as an output of one of said stages;

a logic circuit that generates an enable signal in synchronism with said second internal clock signal and a latch signal in synchronism with said first internal clock signal; and

a memory section that performs one of a read and write operation of data in response to said enable signal and latches said data for one of input and output to said memory section in response to said latch signal.